Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

1. (Currently Amended) A multi-layer integrated semiconductor structure, comprising:

(a) ~~at least~~ a first device layer including:

a first substrate having provided therein a first plurality of doped regions which form at least part of one or more semiconductor elements;

a dielectric material disposed over the first substrate; and

~~a first insulating layer disposed over the first device layer and including at least a first via hole;~~

~~a first conductive plug disposed in the first via hole;~~

a first conductive via provided in the dielectric material, the first conductive via having a first end and a second end;

(b) a ~~first~~ conductive interface ~~portion~~ having a first surface disposed over at least a portion of the first device layer such that at least a portion of the conductive interface is coupled to at least a portion of the first end of the first conductive ~~plug~~via in the first device layer;

(c) ~~at least~~ a second device layer disposed over a second surface of the conductive interface, the second device layer including:

a second substrate having provided therein a second plurality of doped regions which form at least part of one or more semiconductor elements;

~~and including a second via hole~~an insulating material having a surface disposed against a second surface of the conductive interface; ~~and a second conductive plug disposed in the second via hole,~~ wherein the second device layer is secured ~~coupled~~ to the first device layer via the ~~first~~ conductive interface; and

a second conductive via provided in the second device layer having a first end coupled to the conductive interface and having a second end coupled to at least one of the second plurality of doped regions such that ~~portion and wherein the first interface portion provides~~ an electrical ~~a~~ communication path ~~relationship~~ between the first device layer

and the second device layer is provided by the first conductive via, the conductive interface and the second conductive via.~~:~~

2. (Currently Amended) The multi-layer integrated semiconductor structure of claim 1 further comprising a first conductive interconnect element disposed in the dielectric ~~first insulating layer~~material of the first device layer with a first end of the first conductive interconnect element coupled to ~~and wherein~~ the first conductive via and a second end of the first conductive interconnect element coupled to at least one of the first plurality of doped semiconductor elements~~via hole is provided in the first insulating layer to expose at least a portion of the first conductive interconnect element~~.

3. (Cancel)

4. (Currently Amended) The multi-layer integrated semiconductor structure of claim 3~~,~~ further comprising a second conductive interconnect having a first portion disposed over at least a portion of one of the second plurality of doped regions and having a second portion coupled to the second end of ~~wherein~~ the second conductive via~~via hole is formed on a bottom surface of the second device layer and exposes a portion of at least one element of the second plurality of semiconductor elements~~.

5. (Currently Amended) The multi-layer integrated semiconductor structure of claim 1, further comprising a second conductive interconnect disposed in the second device layer and coupled to the second conductive via provided in ~~wherein the second via hole is formed on a top surface of~~ the second device layer ~~and exposes a portion of at least one element of the second plurality of semiconductor elements~~.

6. (Currently Amended) The multi-layer integrated semiconductor structure of claim 5, wherein the second conductive interconnect ~~plug includes a first end~~ is coupled to at least one ~~element~~ of the one or more ~~second plurality of~~ semiconductor elements ~~coupled to at least one element of the second plurality of semiconductor elements and a second end coupled to at least a portion of a second interface portion disposed on the top surface~~of the second device layer.

7. (Currently Amended) The multi-layer integrated semiconductor structure of claim 14, wherein the second conductive via ~~plug~~ includes a first end coupled to the at least one ~~element~~ of the ~~second plurality of~~one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface ~~portion~~.

8. (Currently Amended) The multi-layer integrated semiconductor structure of claim 7~~3~~, wherein ~~via hole is formed on a bottom surface of~~ the second device layer ~~and exposes a portion of~~comprises a second conductive interconnect having a first portion coupled to the second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive via to the at least one element of the second plurality of semiconductor elements..

9. (Currently Amended) The multi-layer integrated semiconductor structure of claim 8 further comprising a third conductive interconnect disposed over at least a portion of the first conductive interconnect with and, wherein the second ~~conductive plug includes a first~~end of the first conductive via is coupled to the first ~~first~~ third conductive interconnect~~interface portion~~.

10. (Currently Amended) The multi-layer integrated semiconductor structure of claim ~~3~~9 further comprising a third conductive via provided in the first device layer, wherein the ~~second~~ third conductive via is coupled between a portion of the ~~via hole is formed on a top surface of the second device layer and exposes a portion of at least a second~~ first conductive interconnect and the at least one of the first plurality of doped regions.

11. (Currently Amended) The multi-layer integrated semiconductor structure of claim 10 further comprising a second conductive interface disposed over a first surface of the second device layer and, wherein the second conductive ~~plug includes a first end coupled to~~via forms at least a part of an electrical communication path between the second conductive interconnect and ~~a second end coupled to~~ at least a portion of athe second interface ~~portion disposed on the top surface of the second device layer~~.

12. (Currently Amended) The multi-layer integrated semiconductor structure of claim 1, wherein the first conductive via forms at least a portion of a signal path between the conductive interface and ~~via-hole exposes a portion of~~ at least one ~~element~~ of the first and second plurality of semiconductor elements.

13. (Currently Amended) The multi-layer integrated semiconductor structure of claim 12, wherein the second end of the first conductive via ~~plug includes a first end~~is coupled to the at least one element of the first plurality of semiconductor elements ~~and a second end coupled to the first interface portion~~.

14. (Currently Amended) The multi-layer integrated semiconductor structure of claim 1, wherein the first conductive interface ~~portion includes a conductive material~~comprises copper.

15. (Currently Amended) The multi-layer integrated semiconductor structure of claim 14 wherein the conductive interface is provided as a first conductive interface region and the multi-layer integrated semiconductor structure further comprises~~, further including~~ a second conductive interface region ~~portion~~ disposed between the first and second device layers with the second conductive interface region being physically separated from the first conductive interface region.

16. (Currently Amended) The multi-layer integrated semiconductor structure of claim 15, wherein the second interface ~~portion~~ region includes an adhesive material such that the second interface region secures the first device layer to the second device layer.

17. (Currently Amended) A multi-layer integrated semiconductor structure, comprising:

at least a first device layer having first and second opposing surfaces, said first device layer including at least a first doped semiconductor region; and a first dielectric material~~insulating layer~~ disposed ~~over~~ about the first doped semiconductor region, said dielectric material having ~~device layer and including~~ at least a first via-hole; with a first conductive material disposed ~~in the first via-hole~~therein to provide a first conductive via having first and second opposing ends; and

~~an interface portion disposed over at least the first conductive material;~~

at least a second device layer having first and second opposing surfaces, said second device layer including at least a second doped semiconductor region and including a second via-hole~~; and~~ having a second conductive material disposed ~~in the second via-hole~~therein to provide a second conductive via having first and second ends ~~;~~;

a first interface disposed between a first one of the first and second opposing surfaces of the first device layer and a first one of the first and second opposing surfaces of the second device layers such that the first interface secures together the first and second device layers and also electrically couples the first device layer to ~~wherein~~ the second device layer ~~is coupled to the first device layer via the interface portion and~~ wherein the conductive interface ~~portion provides~~ and the first and second conductive vias form at least a portion of an electrical communication path ~~relationship~~ between the first device layer and the second device layer.

18. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17 further comprising a first conductive interconnect element disposed in the first ~~insulating~~ device layer ~~and wherein the first via-hole is formed on the first insulating layer and~~ with a first portion of the first conductive via electrically coupled to ~~exposes~~ at least a portion of the first conductive interconnect element and a second portion of the first conductive interconnect element coupled to the first doped semiconductor region.

19. (Currently Amended) The multi-layer integrated semiconductor structure of claim 18, wherein the first conductive via ~~material includes a first end coupled to~~ couples the first conductive interconnect element ~~and a second end coupled~~ to the first conductive interface ~~portion~~.

20. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17, wherein the second conductive via ~~via-hole~~ is formed on ~~a bottom surface~~the first one of the first and second opposing surfaces of the second device layer and is coupled to ~~exposes a portion of~~ the second doped semiconductor region.

21. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17

further comprising a third conductive via coupled to~~, wherein the second via-hole is formed on a top surface of the second device layer and exposes a portion of~~ the second doped semiconductor region.

22. (Currently Amended) The multi-layer integrated semiconductor structure of claim 21 further comprising a second conductive interface disposed on the second one of the first and second opposing surfaces of the second device layer and wherein the third conductive via is provided having ~~, wherein the second conductive material includes~~ a first end coupled to the second doped semiconductor region and a second end coupled to ~~another~~ the second conductive interface ~~portion disposed on the top surface of the second device layer~~.

23. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17, wherein the second conductive via~~via hole~~ is formed on ~~a bottom surface~~ the first one of the first and second opposing surfaces of the second device layer and wherein the second device layer further comprises a ~~exposes a portion of a~~ first conductive interconnect.

24. (Currently Amended) The multi-layer integrated semiconductor structure of claim 23, wherein the second conductive via is provided having~~material includes~~ a first end coupled to the first conductive interconnect and a second end coupled to the first conductive interface~~portion~~.

25. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17, wherein the first conductive via is coupled to at least ~~via hole exposes a portion of~~ the first doped semiconductor region.

26. (Currently Amended) The multi-layer integrated semiconductor structure of claim 25, wherein the first conductive via is provided having ~~material includes~~ a first end coupled to at least the first doped semiconductor region and a second end coupled to the first conductive interface~~portion~~.

27. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17, wherein the first interface corresponds to a first conductor interface region and the multi-layer

integrated semiconductor structure further comprises a second ~~, wherein the~~ interface region disposed between the first one of the first and second device layers with the second interface region provided from a non-conductive ~~portion includes a conductive~~ material.

28. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17, wherein the first conductive interface region is provided from a conductive bonding material~~material includes a first conductive plug~~.

29. (Currently Amended) The multi-layer integrated semiconductor structure of claim 18~~17~~, further comprising a second conductive interconnect element disposed in the second device layer with a portion of the second conductive interconnect element coupled to the second conductive via and wherein the first conductive via, the first conductive interface and the second conductive via provide a direct vertical electrical connection between the first conductive interconnect element and the second conductive interconnect element~~second conductive material includes a second conductive plug~~.

30. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.

31. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.

32. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element.

33. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element.

34. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.

35. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.

36. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area differs from the second predetermined surface area.

37. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area which ~~whereby the first predetermined surface area is~~ is substantially equivalent to the ~~second~~ first predetermined surface area.

38. (Currently Amended) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer ~~includes a first predetermined geometry.~~ further comprises:

a first conductive interconnect element having a first portion coupled to the first doped semiconductor region, and a second portion coupled to a first end of the first conductive via.

39. (Currently Amended) The multi-layer integrated semiconductor structure of claim 38~~17~~, wherein the second device ~~layer includes a second predetermined geometry.~~ further comprises a second conductive interconnect element having a first portion coupled to the second doped semiconductor region and a second portion coupled to a first end of the second conductive via with the second end of the first conductive via and the second end of the second conductive via each coupled to the first interface.

40. (Currently Amended) A multi-layer semiconductor structure, comprising:

a first semiconductor wafer including a first plurality of semiconductor structures each of which includes a first plurality of semiconductor elements;

a second semiconductor wafer including a second plurality of semiconductor structures each of which includes a second plurality of semiconductor elements; and

at least a first conductive bonding interface segment disposed between the first and second semiconductor wafers, said first conductive bonding interface segment disposed over at least a first one ~~semiconductor structure~~ of the plurality of semiconductor structures of the first semiconductor wafer and being in an electrical communication relationship with at least a first one of the first plurality of the semiconductor elements~~element~~ of the first semiconductor structure and~~; at least a second semiconductor structure including a plurality of semiconductor elements being coupled to the first semiconductor structure via the first conductive bonding interface segment, wherein the first conductive bonding interface segment is in an electrical communication relationship with~~ at least a ~~second semiconductor element~~ first one of the plurality of semiconductor elements of the second semiconductor structure of the second semiconductor wafer where the first conductive bonding interface segment permits ~~for permitting~~ at least the first semiconductor element of the first semiconductor structure to communicate with at least the second semiconductor element of the second semiconductor structure~~, via the first conductive bonding interface segment~~.

41. (Currently Amended) A multi-layer semiconductor structure, comprising:

at least a first semiconductor structure including a first plurality of conductive elements;

at least a second semiconductor structure including a second plurality of conductive elements;

a first plurality of conductive bonding interface segments disposed between ~~over~~ the first and second semiconductor ~~structure~~structures with ~~and~~ each of the plurality of conductive bonding interface segments being in an electrical communication relationship with one or more of the conductive elements of the first semiconductor structure and one or more of the conductive elements of the second semiconductor structure~~; at least a second semiconductor structure including a second plurality of conductive elements and being coupled to the first semiconductor structure via at least a first segment of the plurality of conductive bonding interface segments;~~

at least a third semiconductor structure including a third plurality of conductive elements; and

a second plurality of conductive bonding interface segments disposed between the second and third semiconductor structures with each of the second plurality of conductive bonding interface segments being in an electrical communication relationship with one or more of the conductive elements of the second semiconductor structure and one or more of the conductive elements of the third semiconductor structure ~~and being coupled to the first semiconductor structure via at least a second segment of the plurality of conductive bonding interface segments, wherein the first plurality of conductive elements of the first semiconductor structure, the second plurality of conductive elements of the second semiconductor structure and the third plurality of conductive elements of the third semiconductor structure are constructed and arranged to inter-communicate via the first and second segments of the plurality of conductive bonding interface segments~~.